Please type a plus sign inside this box ⊞ PTO/SB/05 (12/97) Approved for use through 09/30/00, OMB 0651-0032

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	04645.0416
Total Pages	22
First Named Inventor or Application Identifier	Barry C. Muffoletto et al.
Express Mail Label No.	EK356002734US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ■ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ■ Specification [*Total Pages* / 12 /]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R&D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ■ Drawing(s) *(35 USC 113)* [*Total Sheets* / 5 /]

4. ■ Oath or Declaration [*Total Pages* / 5 /]
a. ■ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))

9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations

12. ■ Preliminary Amendment

13. ■ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. ☐ Small Entity ☐ Statement filed in prior application, Statement(s) Status still proper and desired

15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)

16. ■ Other: fee transmittal form, check for $690.00 for filing fee

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
☐ Continuation ■ Divisional ☐ Continuation-in-part (CIP) of the prior application No: 09/174,132

18. CORRESPONDENCE ADDRESS

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Martin G. Linihan
Name

Martin G. Linihan
Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Barry C. Muffoletto et al.

A division of Serial No. 09/174,132
Filed October 16, 1998

For: Method For Improving Electrical Conductivity Of Metals, Metal Alloys and Metal Oxides

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Upon the granting of a serial number and filing date to the above-identified divisional application, please amend the application as follows:

In The Claims:

Please cancel claims 1-5.

Respectfully submitted,

HODGSON, RUSS, ANDREWS, WOODS & GOODYEAR, LLP

By _____
Martin G. Linihan
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July 28, 2000
BFLODOCS:419318_1 (8ZJQ01)

BFLODOCS:416168_W)

METHOD FOR IMPROVING ELECTRICAL CONDUCTIVITY OF METALS, METAL ALLOYS AND METAL OXIDES

Background of the Invention

This invention relates to the art of treating metals, metal alloys and metal oxides, and more particularly to a new and improved method for enhancing the electrical conductivity of metals, metal alloys and metal oxides.

One area of use of the present invention is in the manufacturing of electrodes for capacitors, batteries and the like, although the principles of the present invention can be variously applied. Metals and metal alloys have a native oxide present on the surface. This is an insulating layer and hence if the material is to be used as a substrate for an electrode, the oxide has to be removed or made electrically conductive.

If the oxide is removed by chemical treatment, such as by etching with an acid or electrolytic etching to expose the underlying metal, special steps must be taken in order to complete the electrical contacts before the native oxide can be regenerated and interfere with the electrical contacts. Such measures require special apparatus and extremely careful handling of the materials, all of which adds cost to the fabricating of electrical devices incorporating these materials to which electrical contact must be made. Another approach involves removing the oxide layer and plating the bare substrate metal with an expensive noble metal, such as silver, gold, or alloys of silver, gold and platinum, or the formation of an electrically conducting compound on the bare substrate surface. The materials employed are expensive and the steps required to plate the substrate are costly and time consuming. In addition, the metal plating or electrically conducting compound must be disposed on the substrate as a continuous film for maximum performance. Therefore, the plating or compound formation typically is carried out after the substrate metal is formed into its final shape for

the electrical device in which it is incorporated in order to avoid damage to the coating. This, in turn, adds to the cost and complexity of the manufacturing process.

United States Patent 5,098,485 issued March 24, 1992 to David A. Evans proposes a solution to the oxide problem by altering the native oxide from an electrically insulating to an electrically conducting condition without removal of the native oxide layer to expose the underlying metal or alloy. A solution containing ions of an electrical material is applied to the native oxide layer, and then the substrate, oxide and applied ions are heated to an elevated temperature for a time sufficient to incorporate the ions into the oxide layer to change it from an electrical insulator to an electrical conductor.

Summary of the Invention

It would therefore, be highly desirable to provide a new and improved method for enhancing the electrical conductivity of metals, metal alloys and metal oxides which does not require additional heat treatment, which provides control over the density and depth of the material introduced to the treated surface, which can be performed in a manner preventing substrate degradation and deformation, and which improves the quality of the treated surface.

The present invention provides a method for improving the electrical conductivity of a substrate of metal, metal alloy or metal oxide which includes depositing a small or minor amount of metal or metals from Group VIIIA metals (Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt) or from Group IA metals (Cu, Ag, Au) on a substrate of metal, metal alloys and/or metal oxide from Group IVA metals (Ti, Zr, Hf), Group VA metals (V, Nb, Ta), Group VIA

metals (Cr, Mo, W) and Al, Mn, Ni and Cu. The native oxide layer is changed from electrically insulating to electrically conductive. The depositing process is a low temperature arc vapor deposition process. This may be done in a deposition chamber. The deposition may be performed on either treated or untreated substrate. After deposition the substrate is available for use as a substrate and no other processing steps may be necessary.

The method of the present invention advantageously does not require additional heat treatment and provides control over the density and depth of the material introduced onto the treated surface thereby not affecting the bulk of the material. The method can be performed at a temperature sufficiently low so as to prevent substrate degradation and deformation. It is believed that the quality of the treated surface is improved by the method of the present invention. Multiple processing steps may be incorporated into the method, for example substrate cleaning, oxide removal and etching. Another advantage is that using a substrate treated by the method of the present invention will allow the surface thereof to be treated to passivate it from chemical reaction while still providing adequate electrical conductivity. Stainless steels having native insulating oxide layers also can be treated by the method of the present invention to provide an electrically conductive oxide layer.

A substrate treated by the method of the present invention is ready for further processing in the manufacture of an electrode for use in capacitors, batteries and the like. Typically, in the case of a capacitor, an appropriate electrode material is deposited on the substrate treated surface by techniques well-known to those skilled in the art. Examples of electrode materials are redox pseudo capacitance materials such

as, but not limited to, oxides and mixed oxides of ruthenium, iridium, manganese, nickel, cobalt, tungsten, niobium, iron, molybdenum or double layer materials or under potential deposition materials such as palladium, platinum, lead dioxide or electro-active conducting polymers such as polyaniline, polypyrole and polythiophene.

The foregoing and additional advantages and characterizing features of the present invention will become clearly apparent upon a reading of the ensuing detailed description together with the included drawing wherein:

Brief Description of the Drawing Figures

Fig. 1 is a diagrammatic view illustrating the method of the present invention at one stage thereof;

Fig. 2 is a diagrammatic view illustrating the method of the present invention at another stage thereof;

Fig. 3 is a diagrammatic view of a substrate after treatment by the method of the present invention;

Fig. 4 is a diagrammatic view of the substrate of Fig. 3 having electrode material deposited thereon for use in manufacture of a capacitor electrode; and

Figs. 5-7 are graphs depicting impedance spectroscopy scans on substrates of the type shown in Fig. 4.

Detailed Description of the Illustrated Embodiment

Metals and metal alloys have a native oxide present on the surface which is electrically insulating and must be removed or made electrically conductive if the metal or metal alloy is to be used as an electrode in devices such as capacitors and batteries. Referring to Fig. 1 there is shown a substrate 10 having an electrically insulating native oxide layer 12 on a surface thereof. In accordance with the present invention, oxide layer 12 is made more electrically conductive, i.e. changed from electrically insulating to electrically conductive. Substrates treated by the method of the present invention include metals and alloys thereof selected from the group consisting of Group IVA metals (Ti, Zr, Hf), Group VA metals (V, Nb, Ta), Group VIA metals (Cr, Mo, W), aluminum, manganese, nickel, copper and stainless steel. They typically have a thickness in the range from about 0.001 mm. to about 2.0 mm.

In accordance with the present invention, a layer 14 is deposited on the native oxide layer 12 wherein the layer 14 is a small amount of metal or metals selected from the group consisting of Group IA metals (Cu, Ag, Au) and Group VIIIA metals (Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt). The layer 14 is deposited by a low temperature arc vapor deposition process (LTAVD). As shown in Fig. 2, the process represented diagrammatically by dotted line 20 is carried out by apparatus 22. The deposition may be performed on either treated or untreated substrate, and the deposition may or may not be preceded by removal of the oxide from the substrate. This may be done in the deposition chamber of apparatus 22. The native oxide layer 12 is changed from electrically resistive to electrically conductive. After deposition the substrate is available for use as a substrate and no other processing steps may be necessary.

The depositing of metal 14 on native oxide layer 12 by means of the low temperature are vapor deposition process 20 converts the electrically insulating native oxide layer 12 to a mixed layer 30 on substrate 10 as shown in Fig. 3 which mixed layer 30 has a degree of electrical conductivity sufficient to make substrate 10 useable as an electrode in a device such as a capacitor or battery. In other words, native oxide layer 12 has been converted from being essentially non-conductive, i.e. insulating, to having an increased and improved degree of electrical conductivity. Thus, the quality of the treated surface of substrate 10 is improved in that the surface layer 12 is changed from an insulating, semiconducting or dielectric state to an electrically conducting state.

The substrate shown in Fig. 3, treated by the method of the present invention, is ready for further processing in the manufacture of an electrode for use in capacitors, batteries and the like. Typically, in the case of a capacitor, an appropriate electrode material 40 as shown in Fig. 4 is deposited on the substrate treated surface by techniques well-known to those skilled in the art. Examples of electrode material 40 are redox pseudo capacitance materials such as, but not limited to, oxides and mixed oxides of ruthenium, iridium, manganese, nickel, cobalt, tungsten, niobium, iron, molybdenum, or under potential deposition systems such as palladium, platinum, lead dioxide or electro-active conducting polymers such as polyaniline, polypyrole, and polythiophene.

The present invention is illustrated further by the following example.

Example

A tantalum or titanium substrate similar to substrate 10 shown in Fig. 1 is first abraded on one side using a 3M Scotch-brite pad of very fine type. This produces a rough surface on the side to be coated. It is then degreased and cleaned. This is accomplished by cleaning the foil in an ultrasonic bath using acetone as a solvent for 10 minutes. Next it is washed in an ultrasonic methanol bath and then blow dried using dry, clean compressed air.

The substrate is now ready to be coated with palladium. It is placed in a Low Temperature Arc Vapor Deposition (LTAVD) apparatus similar to apparatus 22 of Fig. 2 to be coated. After the sample is loaded into the apparatus the pressue in the deposition chamber is lowered by a vacuum pump to 10^{-5} - 10^{-6} Torr. This gets rid of all waste gases, specially oxygen. In this process oxygen is a contaminant. The pressue is brought up to the mTorr range by introducing argon into the chamber. The substrate is biased to 600V and an arc is struck. This arc is now used to remove the native oxide layer on the tantalum. On completion of the oxide removal the bias voltage is reduced to 50-100V. The palladium is evaporated, by the arc, from the electrode and coats the substrate. The coating thickness is about 0.1 micron. After the deposition is complete the chamber is back filled with argon and brought back to atmospheric pressure. The substrate is now ready to be coated with ruthenium oxide, as the coating provides good electrical contact to the bulk tantalum, for use in making a capacitor electrode.

Figs. 5-7 depict impedance spectroscopy scans on substrates treated according to the present invention and coated with ruthenium oxide for use as capacitor electrodes. Fig. 5 compares the capacitance of the ruthenium oxide coating on bare

tantalum to capacitance of the ruthenium oxide coating on tantalum treated according to the present invention. Curve 50 in Fig. 5 is for bare or unprocessed tantalum, and curve 52 is for tantalum treated according to the present invention by the LTAVD process 20. The relatively lower capacitance of the untreated tantalum is due to the presence of the insulating native oxide.

Fig. 6 compares the resistance of the ruthenium oxide coating on bare tantalum to resistance of the ruthenium oxide coating on tantalum treated according to the present invention. Curve 58 in Fig. 6 is for bare or untreated tantalum, and curve 60 is for tantalum processed according to the present invention using the LTAVD process 20. The relatively higher resistance of the untreated tantalum at the lower end of the frequency spectrum is due to the presence of the insulating native oxide. Fig. 7 shows the coating behavior with unprocessed tantalum in curve 64, and tantalum processed according to the present invention in curve 66, using LTAVD process 20.

Table I presents additional capacitance and resistance data from Figs. 6 and 7 comparing untreated tantalum with a ruthenium oxide coating to ruthenium oxide coated tantalum treated according to the present invention using the LTAVD process 20.

Table I

Tantalum Material	Cs	Rs
Bare Tantalum coated with Ru Oxide	22.30 mF/sq in	521.26 m ohm
Tantalum-LTAVD process coated with Ru Oxide	473.38 mF/sq in	28.56 m ohm

It is therefore apparent that the present invention accomplishes its intended objects. While embodiments of the present invention have been described in detail, that is for the purpose of illustration, not limitation.

What is claimed is:

The Claims

1. A method of improving electrical conductivity of metals, metal alloys and metal oxides comprising:

a) providing a substrate having an electrically insulating native oxide layer on a surface thereof, said substrate being selected from the group consisting of Group IVA, Group VA and Group VIA metals, aluminum, manganese, nickel, copper and stainless steel; and

b) utilizing a low temperature arc vapor deposition process to deposit on said native oxide layer a metal selected from the group consisting of Group IA and Group VIIIA metals;

c) whereby said native oxide layer is changed from being electrically insulating to being more electrically conductive.

2. A method according to claim 1, including sequentially depositing and intermixing until a predetermined mixing depth is obtained.

3. A method according to claim 1, further including applying a coating on said native oxide layer whereby said substrate is useable as an electrode in a capacitor.

4. A method of improving electrical conductivity of metals, metal alloys and metal oxides comprising:

a) providing a substrate having an electrically insulating native oxide layer on a surface thereof, said substrate being of a material operative for use as an electrode in a capacitor; and

b) utilizing a low temperature arc vapor deposition process to deposit on said substrate surface a metal selected from the group consisting of Group IA and Group VIIIA metals;

c) whereby said native oxide layer is changed from being electrically insulating to being more electrically conductive.

5. A method according to claim 4, further including applying a coating of capacitor electrode material on said native oxide layer.

6. A substrate of improved electrical conductivity wherein said substrate is selected from the group consisting of Group IVA, Group VA and Group VIA metals, aluminum, manganese, nickel, copper and stainless steel and said substrate having a native oxide layer on a surface thereof, and wherein said sustrate surface has deposited thereon metal selected from the group consisting of Group IA and Group VIIIA metals for increasing the electrical conductivity of said native oxide layer.

7. A substrate according to claim 6 further including a coating on said native substrate surface of material rendering said substrate useable as an electrode in a capacitor.

Abstract

A method for improving the electrical conductivity of a substrate of metal, metal alloy or metal oxide comprising depositing a small or minor amount of metal or metals from Group VIIIA metals (Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt) or from Group IA metals (Cu, Ag, Au) on a substrate of metal, metal alloys and/or metal oxide from Group IVA metals (Ti, Zr, Hf), Group VA metals (V, Nb, Ta), Group VIA metals (Cr, Mo, W) and Al, Mn, Ni and Cu. The native oxide layer of the substrate is changed from electrically insulating to electrically conductive. The step of depositing is carried out by a low temperature arc vapor deposition process. The deposition may be performed on either treated or untreated substrate. The substrate with native oxide layer made electrically conductive is useable in the manufacture of electrodes for devices such as capacitors and batteries.

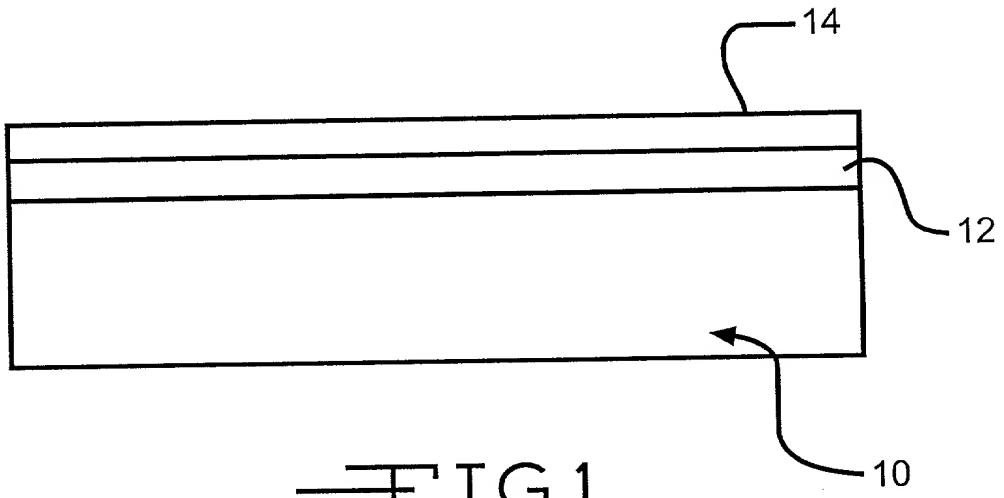


FIG.1

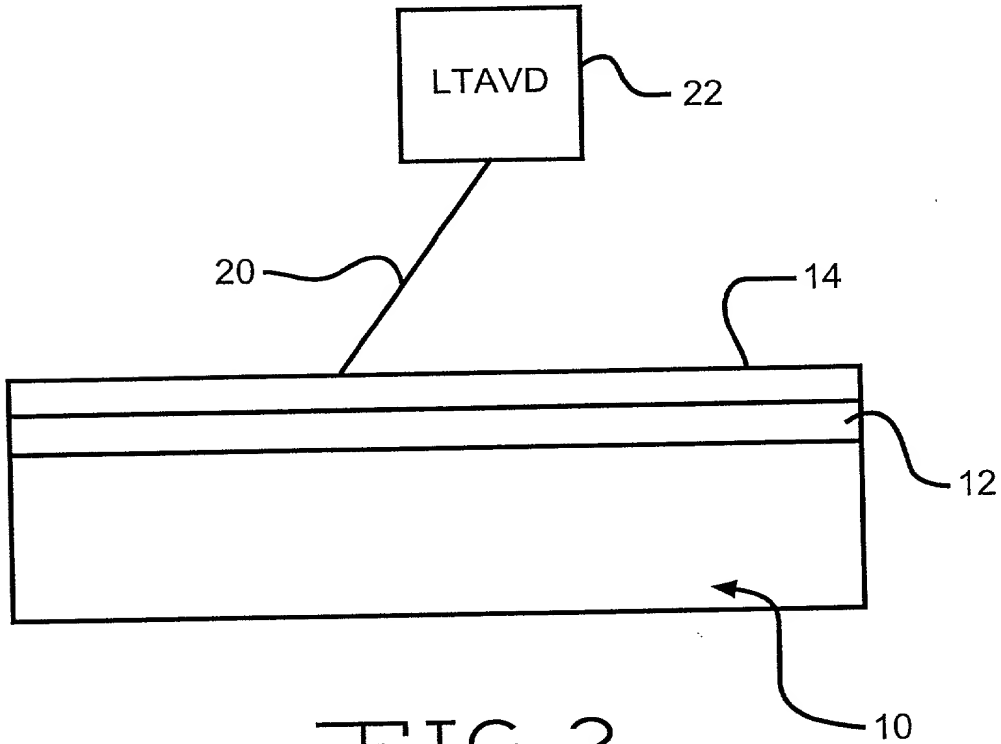


FIG. 2

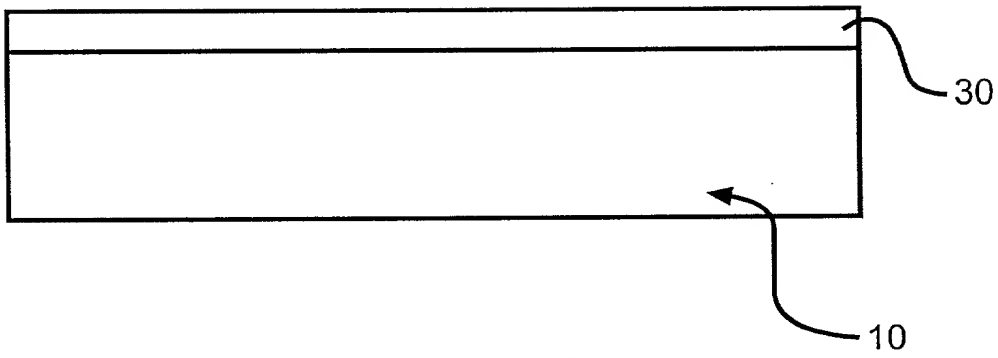


FIG. 3

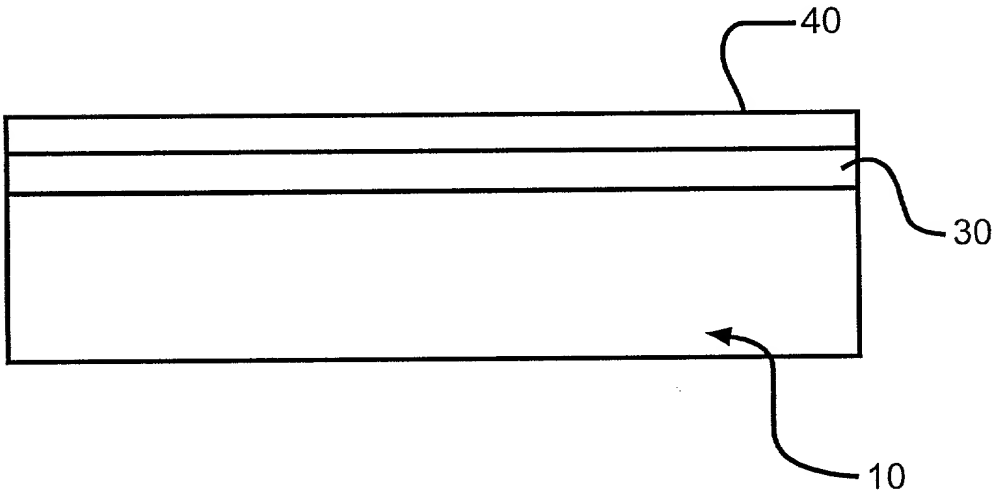
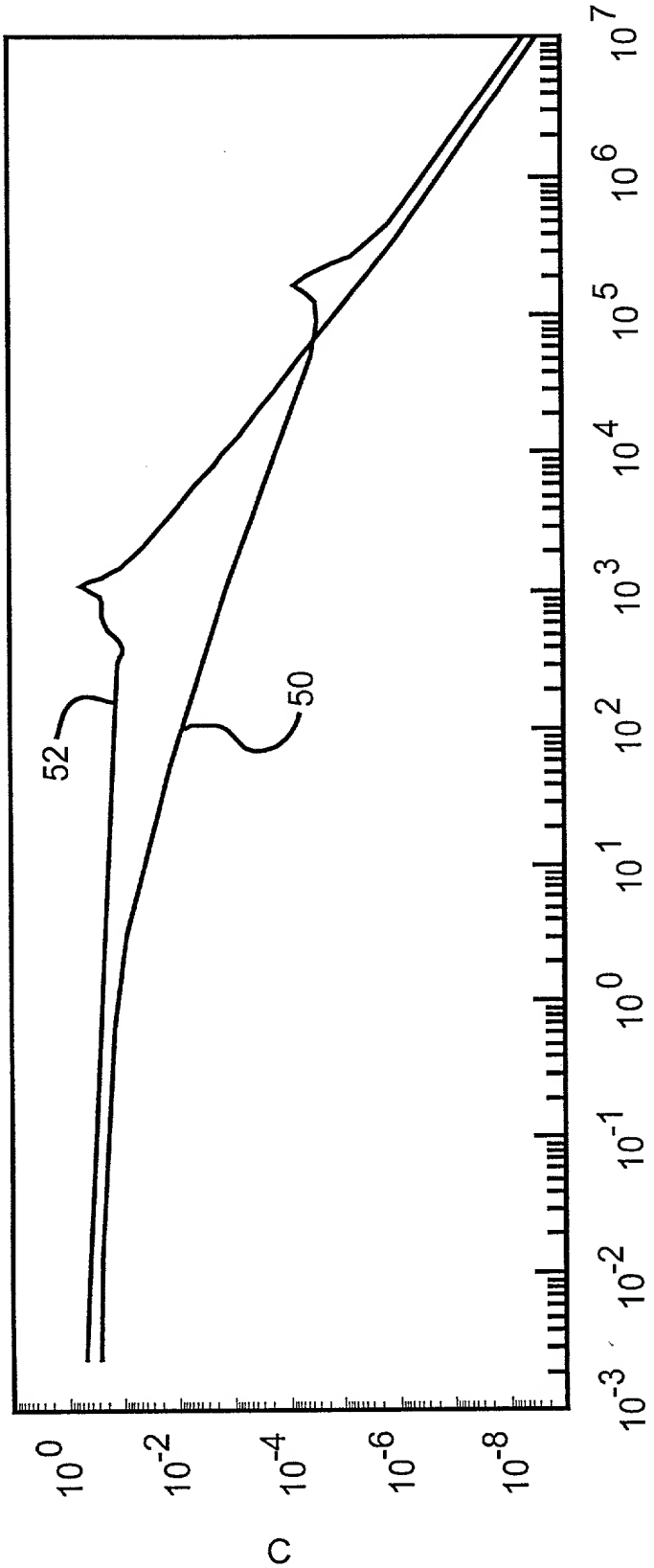


FIG. 4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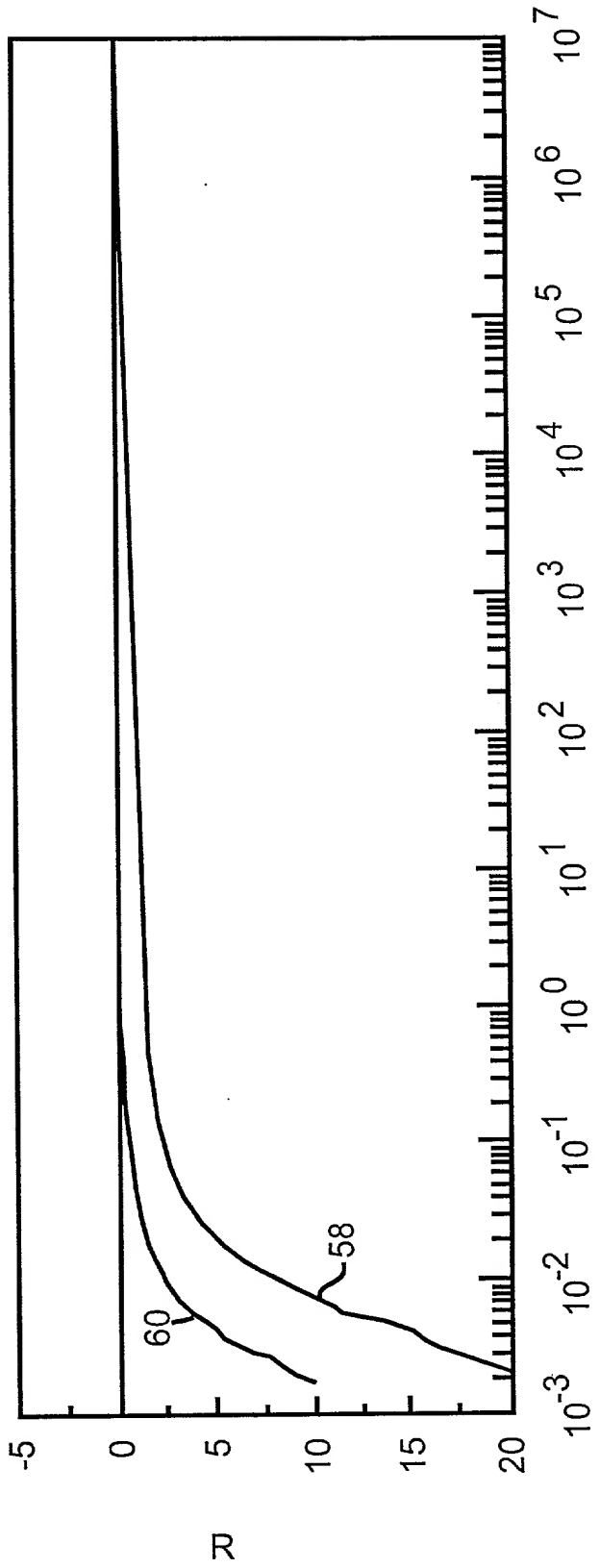
FREQUENCY (Hz)

FIG. 5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FREQUENCY (Hz)
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58

FIG.6

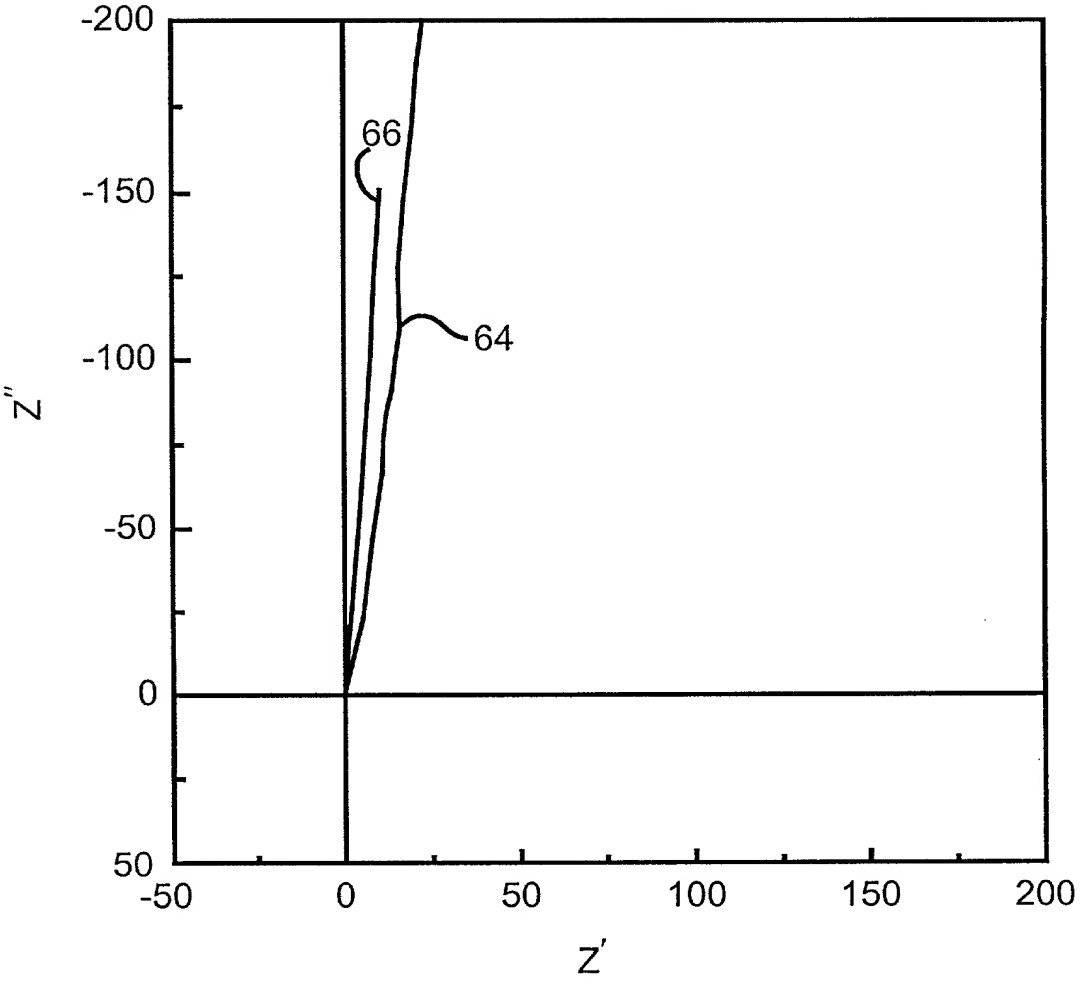

FIG. 7

Attorney's Docket No. 04645.0416

PATENT

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR CIP)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: (check one applicable item below)

/X/ original

/_/ design

/_/ supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation in-part application do not check next item; check appropriate one of last three items.

/_/ national stage of PCT

NOTE: If one of the following 3 items apply then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR CIP.

/_/ divisional

/_/ continuation

/_/ continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

METHOD FOR IMPROVING ELECTRICAL CONDUCTIVITY OF METALS, METAL ALLOYS AND METAL OXIDES

SPECIFICATION IDENTIFICATION

the specification of which: (complete (a), (b) or (c))

(a) /X/ is attached hereto.

(b) /_/ was filed on _____ as /_/ Serial No. 0 /_____ or /_/ Express Mail No., as Serial No. not yet known _____ and was amended on _____ (if applicable).

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) /_/ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____ (if any).

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information

- which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56.

(also check the following items, if desired)

/_/ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent, and

/_/ In compliance with this duty there is attached an information disclosure statement in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. § 119)

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) /X/ no such applications have been filed.

(e) /_/ such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. claimed priority check item (e), enter the details below and make the priority claim.

A. PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

COUNTRY (OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			/ / YES NO / /
			/ / YES NO / /
			/ / YES NO / /
			/ / YES NO / /
			/ / YES NO / /

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CIP APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

Martin G. Linihan	Reg. No. 24,926
Edwin T. Bean, Jr.	Reg. No. 16,639
Michael F. Scalise	Reg. No. 34,920
Ranjana Kadle	Reg. No. 40,041
Kevin McCarthy	Reg. No. 35,278
John Del Vecchio	Reg. No. 42,475
Maria M. Eliseeva	Reg. No. 43,328
Daniel C. Oliverio	Reg. No. 33,435

(check the following item, if applicable)

/_/ Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO

HODGSON, RUSS, ANDREWS, WOODS & GOODYEAR
INTELLECTUAL PROPERTY PRACTICE GROUP
1800 ONE M & T PLAZA
BUFFALO, NY 14203-2391

DIRECT TELEPHONE CALLS TO
(Name and telephone number)

(716) 856-4000

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Full name of **sole or first inventor** Barry C. Muffoletto

(GIVEN NAME) MIDDLE INITIAL OR NAME FAMILY (OR LAST NAME)

Inventor's signature Barry C Muffoletto

Date 07 oct 98 Country of Citizenship United States

Residence 11747 Buckwheat Road, Alden, New York 14004

Post Office Address same as above

Full name of **second joint inventor,** if any Ashish Shah

(GIVEN NAME) MIDDLE INITIAL OR NAME FAMILY (OR LAST NAME)

Inventor's signature Ashish Shah

Date 07 OCT. 98 Country of Citizenship United States

Residence 10 San Pablo Court, East Amherst, New York 14051

Post Office Address same as above

CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGE(S) WHICH FORM A PART OF THIS DECLARATION

/ / Signature for third and subsequent joint inventors. Number of pages added _____.

/_/ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. Number of pages added _____.

/_/ Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. Number of pages added _____.

* * *

/_/ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (CIP) application.

/_/ Number of pages added _____.

* * *

/_/ Authorization of attorney(s) to accept and follow instructions from representative.

* * *

If no further pages form a part of this Declaration then end this Declaration with this page and check the following item

/X/ This declaration ends with this page